Remarks

Upon entry of the foregoing amendment, claims 1-5 and 8-15 are pending in the application, with claims 1 and 11 being the independent claims. Claims 1 and 11 are amended to increase their clarity. New claims 14 and 15 are added for examination. No new matter is entered by these changes.

Based on the above amendment and the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Interview Summary

The courtesy extended to applicant's representative by Examiner Tonia Meonske in the interview of March 7, 2005 is noted with appreciation. During the interview, the citations in the Office Action were discussed and the Examiner clarified her interpretation of the cited passages of the cited references. It was agreed that applicants would examine the references in light of that clarification, and respond with appropriate arguments.

Rejection under 35 U.S.C. 103

The pending claims were rejected under 35 U.S.C. 103 based on the combination of U.S. Patent 5,996,066 to Yung and U.S. Patent 6,272,514 to Petro et al. This rejection

is respectfully traversed and reconsideration is requested based on the amendments herein and the following remarks.

Yung discloses a graphics processor architecture where pixel data are "packed" into a data path. Yung does not, however, teach or suggest the feature recited in claims 1 and 11 wherein "a prior operation" operates "to set condition values so that, when the operands have less than the maximum number of lanes, two or more condition values are set to a same value so that each individual condition value is generated regardless of a degree of packing of the first and second source operands."

Embodiments exemplifying this feature are described in the present specification starting (for example) at page 2, line 15 and starting at page 12, line 13. In the disclosed embodiments, when an instruction is to be executed on a less densely packed object, condition codes are set corresponding to a maximum packing density regardless of the density actually employed. For example, if there is a maximum capacity of eight lanes, all eight condition codes are set based on the outcome of a prior executed operation, even if there are only one, two or four packed objects in the register. In an exemplary embodiment disclosed in the specification, multiple condition codes applying to a lane are all set to match the value of a calculated condition code for that lane.

Those skilled in the art might have initially dismissed this approach as requiring additional effort and computational time compared to the alternative of providing only one test register and set of condition codes for each lane. However, the inventor discovered that this approach produces a significant unobvious advantage, as described in the specification. That is, once the condition codes have been set in this manner, they are available and can be used in subsequent instructions operating with the same or a different degree of packing.

Similarly, Yung does not disclose or suggest using stored condition information "derived from the results of executing a prior instruction sequence," to determine "independently" for each respective lane whether an instruction should be executed, as further recited in the amended claims. Yung indicates that his instructions may execute conditionally based on mask values (see col. 2 lines 20-22). However, Yung's mask values are not derived from a previous operation; they select movement of data between registers and are disclosed as being set by an instruction (see col. 8 lines 17-18).

As noted in the background section of the specification, predicated execution of instructions is known, but has not been applied independently to different parts of a packed register in the present context and in combination with the feature of setting condition values for a maximum operand density. In an exemplary embodiment of the invention, for example, instructions may execute differently for different lanes in the same register based on one of 16 test conditions derived from a negative, zero, carry, or overflow condition (see table on page 7 of the specification). This feature significantly enhances processing capacity and works in harmony with the recited feature of generating condition values based on the maximum density rather than the density actually in use.

The Petro et al. reference was cited in the Official Action as teaching grouping adjacent ALU's together for parallel operations. The Official Action asserts that it would have been obvious to modify Yung to incorporate the features of Petro et al., and that it "logically follows" that adjacent masks would be grouped in such a combination. During the interview, it was noted that Petro provides hardware that can be adapted to operate on partitioned operands. In particular, Petro discloses selectively disabling bit carries between partitions so that arithmetic operations in one partition do not affect the contents

of another partition. It was suggested in the interview that control signals would be needed in Petro to selectively activate each ALU component, and that those control signals would meet the claim language. After due analysis and consideration, applicant respectfully disagrees.

Petro is substantially silent as to such control signals and provides no clear disclosure of such operations. Further, such control signals, even if they are present in the form assumed by the Examiner, would merely control whether carries for that segment propagate to the next ALU. If such signals were present and operate as asserted by the Examiner, so that eight such signals are present for a 64-bit register (although again, there is no disclosure of same), and indicate whether the carry is to operate, the signals would appear as 01010101 for 16 bit packing, 01110111 for 32-bit packing, etc. That is, carry would be turned on for all but the leftmost segment of each operand.

Carry control signals of this type, as suggested during the interview, are not actually disclosed in the reference, and in any case would not meet the claim terms. The pending claims recite that a number of stored condition values corresponds to the maximum number of lanes, and that a prior operation set those condition values such that when the operands are at less than maximum density, two or more are set to the same value.

The hypothetical carry signals described above are not set in this manner. Among other things, such carry control signals would not constitute "condition values" set by a prior executed operation. The claims have been amended to even more clearly point out this feature. In particular, the independent claims now further recite that stored condition values are derived from the results of executing a prior instruction sequence, and are used to determine independently for each respective lane whether or not an

operation defined in the instruction is to be implemented on that lane of the operand. The signals used to control the circuit of Petro et al., to the extent they are disclosed or suggested by the reference, do not perform these functions.

Thus, the Yung and Petro et al. references do not individually disclose the features of the invention. Further, neither reference remedies the deficiencies of the other with respect to teaching a person of ordinary skill in the art to make and used the claimed invention. Thus, whether taken alone or in combination, upon further analysis these references do not add up to a prima facie case of obviousness.

It should also be noted that a person skilled in the art would not be motivated to combine these references. The Official Action asserts that the combination would be motivated by a desire to provide parallel operation in Yung. However, Yung already provides parallel operation, that is, the ability to operate on multiple pixels at one time. Petro et al. appears merely to disclose a specific logic circuit for an adder that can be partitioned like the one in Yung.

Further, these two references actually teach away from the claimed invention. While both appear to show packing data into a single register to permit faster operations, they provide and use condition values only for the objects and object sizes actually present. Neither reference comes close to suggesting, for example, setting eight condition codes in response to a previous operation when only one or two or four data elements are present. There does not appear to be any reason why Yung or Petro, or a person of ordinary skill reviewing these references, would have decided to add hardware or software logic to store condition codes that are not needed for any operations disclosed in those two references. There is no recognition of the unobvious advantages

provided by that feature, and thus no motivation for a person of ordinary skill to add steps and functions for that purpose.

The feature of setting additional condition values based on the maximum packing even when the operands are packed at a lower density thus runs counter to the specific disclosure of Yung and Petro et al., and to their objectives of maximizing processing speed and minimizing the number of logic operations to be performed.

To make a prima facie case of obviousness, the combination of references must produce the features recited in the claims. Yung does not disclose the feature of generated individual condition values based on a prior operation at maximum density, even when the object is less densely packed, and neither does Petro et al. The assertion that the claimed feature would "logically follow" from such a combination is not supported by the cited references and is respectfully traversed. Neither reference discloses or suggests the above-noted advantages of the claimed invention, nor do they provide any other specific motivation for providing the claimed features.

For the reasons stated, applicants believe that on further review, the office will find that the cited references do not make out a prima facie case of obviousness. To the extent that there may be a prima facie case of obviousness based on these or other references, such case would be overcome by the unobvious advantages of the invention as described in the specification.

Thus, applicants assert that independent claims 1 and 11 and patentable over the cited references for at least these reasons. Dependent claims 2-5, 8-10, 12 and 13, and new claims 14-15, are also patentable over the cited references for at least these reasons, and further in view of their own features.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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